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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/437,579	11/09/99	MACINNIS A	36275/SAH/B6

EXAMINER	
TUNG, K	
ART UNIT	PAPER NUMBER
2776	6

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DATE MAILED: 06/26/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
637,579	Macinnis et al
Examiner	**Group Art Unit**
K. Tung	2776

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Response

A SHORTENED STATUTORY PERIOD FOR RESPONSE IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a response be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for response is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication .
- Failure to respond within the set or extended period for response will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

☐ Responsive to communication(s) filed on 5-31-00.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☑ Claim(s) 1-58 is/are pending in the application.

Of the above claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☑ Claim(s) 1-58 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claim(s) _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 11 9(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 1 7.2(a)).

*Certified copies not received: _____.

Attachment(s)

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☑ Notice of References Cited, PTO-892

☑ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Interview Summary, PTO-413

☐ Notice of Informal Patent Application, PTO-152

☐ Other _____

Office Action Summary

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. Claims 1-5, 19, 23, 25-27, 29-31, 37, 44, 50, 51, 53-56 and 58 are rejected under 35 U.S.C. § 102(e) as being anticipated by Ben-Yoseph et al (5,949,439).

Ben-Yoseph et al teaches a graphics accelerator (Fig. 1) comprising a memory (SRAM 146) for graphics data, the graphics data including pixels; a coprocessor (106) for performing vector type operations on a plurality of components of one pixel of the graphics data (col. 3, lines 11-39). Therefore, at least claims 1 and 2 are anticipated by Ben-Yoseph et al.

As per claim 3, Ben-Yoseph et al teaches a DMA engine for loading the graphics data from memory through loading operations and transferring processed graphics data to the memory through storing operations (col. 4, lines 36-40 and col. 4, line 65 through col. 5, line 4).

As per claims 4 and 5, Ben-Yoseph et al teaches the coprocessor processes the plurality of components of each pixel, RGB components, in parallel as three elements of a vector (inherent by any 3D graphics pixel data which normally in RGB format and YUV for video data).

As per claim 19, Ben-Yoseph et al teaches the coprocessor has an instruction set that includes a special instruction for comparing between each element of a pair of 3-element vectors (inherent by the VLIW, col. 3, lines 35-39).

As per claim 23, Ben-Yoseph et al teaches the DMA engine moves data between the memory and an external memory at the same time the graphics accelerator is using the memory for its load and store operations (col. 4, lines 36-40 and col. 4, line 65 through col. 5, line 4).

As per claim 25, Ben-Yoseph et al teaches the DMA engine includes a queue to hold a plurality of DMA commands (inherent by portion of SRAM 146, col. 5, lines 50-62 and/or software queue 144).

As per claim 26, Ben-Yoseph et al teaches the plurality of DMA commands are executed in the order they are received (inherent by any FIFO buffer and/or software queue 144).

As per claim 27, Ben-Yoseph et al teaches the queue comprises a mechanism that allows the graphics accelerator to determine when all the DMA commands have been completed (read and write pointers 136 and 138, col. 5, lines 26-30).

As per claim 29, Ben-Yoseph et al teaches the graphics accelerator is working on operands and producing outputs for one set of pixels, while the DMA engine is bringing in operands for a future set of pixel operations (inherent by the teachings of FIFO type queue or portions of SRAM of Ben-Yoseph et al and/or software queue 144).

The method claims 30 and 31 are similar in scope to the apparatus claims 1 and 5, and thus are rejected under similar rationale.

As per claim 37, Ben-Yoseph et al teaches each of the plurality of pixels of graphics data comprises YUV components of YUV formatted graphics data (col. 5, lines 5-7).

Claim 44 is similar in scope to claim 19, and thus is rejected under similar rationale.

Claims 50 and 51 are similar in scope to claims 3 and 2, and thus are rejected under similar rationale.

Claims 53-56 and 58 are similar in scope to claims 25, 27, 26 and 29, and thus are rejected under similar rationale.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3, 23-29 and 50-58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ben-Yoseph et al (5,949,439) in view of Gulick et al (5,758,177).

The teachings of Ben-Yoseph et al are given in previous paragraph of this Office action. However, Ben-Yoseph et al fails to explicitly suggest the external memory is a unified memory that is shared by a graphics display system, a CPU and other peripheral devices. This is what Gulick et al teaches (col. 6, lines 39-46 and Fig. 7, 110). Gulick et al further teaches a multimedia digital system chip (112 and/or 112B) comprising a video/graphics engine (202), an audio engine (204), a

general purpose DSP (206), memory buffer (234), DMA engine (236), memory controller logic (604), chipset logic (608), ... It would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teaches of Gulick et al into the system of Ben-Yoseph et al in order to more efficiently use of the memory system because the memory capacity can dynamically allocated based on the request, thus avoid the waste of the memory. Therefore, at least claim 24 would have been obvious.

As per claim 3, Gulick et al teaches a DMA engine for loading the graphics data from memory through loading operations and transferring processed graphics data to the memory through storing operations (DMA engine 236).

As per claim 23, Gulick et al teaches the DMA engine moves data between the memory and an external memory at the same time the graphics accelerator is using the memory for its load and store operations (col. 6, lines 42-46).

As per claim 25, Gulick et al teaches the DMA engine includes a queue to hold a plurality of DMA commands (obvious by the memory buffer 234).

As per claim 26, Ben-Yoseph et al teaches the plurality of DMA commands are executed in the order they are received (also would have been obvious by the memory buffer 234 in FIFO type).

As per claim 27, Gulick et al teaches the queue comprises a mechanism that allows the graphics accelerator to determine when all the DMA commands have been completed (would be obvious by any read and write pointers).

As per claim 28, Gulick et al teaches the queue is four deep for storing up to four DMA commands (would be obvious by any FIFO to configure into any reasonable size (storage capacity)).

As per claim 29, Gulick et al teaches the graphics accelerator is working on operands and producing outputs for one set of pixels, while the DMA engine is bringing in operands for a future set of pixel operations (inherent by the teachings of buffer 234 because this what this buffer for).

Claims 50-58 are similar in scope to claims 3 and 23-29, and thus are rejected under similar rationale.

5. Claims 6-18, 20-22, 32-43, and 45-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ben-Yoseph et al (5,949,439) in view of Hancock (5,604,514).

The teachings of Ben-Yoseph et al are given in previous paragraph of this office action. However, Ben-Yoseph et al fails to explicitly mention the pixels are in an RGB16 format. Ben-Yoseph et al teaches receiving video data in an 16-bit YUV format. It was old and well known and well use in the art that the pixel data can be any format, such as, RGB16, RGB8, RGB24, YUV8, YUV16, or YUV24 etc ... Furthermore, Hancock teaches the pixel data RGB16, YUV16, etc ... (Fig. 3, col. 3, line 52 through col. 4, line 6, col. 5, lines 6-17). It would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of Hancock into the system of Ben-Yoseph et al in order to improve video subsystem fro concurrently displaying graphics and image data as taught by Hancock (col. 2, lines 28-30). Therefore, at least claims 6-8, 13-16, 32-33, 37-40 and 45-46 would have been obvious by Ben-Yoseph et al and Hancock.

As per claim 9, Ben-Yoseph et al teaches the two pixels are respectively selected by two special load instructions (col. 3, lines 57-65).

As per claim 10, Ben-Yoseph et al teaches the two special load instructions are for loading a left one and a right one of the two pixels, respectively (150 and col. 3, lines 35-65).

As per claim 11, Ben-Yoseph et al teaches the coprocessor comprises an input register (SRAM 146).

As per claim 12, the combined system fails to specifically suggest the RGB components are expanded into 8-bit components through zero expansion when loaded into the input register. How, it would have been obvious to one of ordinary skill in the at the time the present invention was made to implement the teachings of MPEG decode of Ben-Yoseph et al and Hancock in order to obtain the claimed feature.

As per claims 17 and 18, Ben-Yoseph et al teaches the two pixels are respectively selected by two special load instructions for extracting a first one and a second one of the two pixels, respectively (150 and col. 3, lines 35-65).

As per claim 20, Ben-Yoseph et al teaches a result register for storing the results of the three comparisons (col. 5, lines 50-62).

As per claim 21, the combined system fails to explicitly teach the results of the three comparisons are used together during a single conditional branch operation. It would have been obvious to one of ordinary skill in the art at the time the present invention was made to implement

the teachings of using VLIW technology and instruction unit of Ben-Yoseph et al in order to increase system processing performance.

As per claim 22, the combined system also fails to explicitly teach the special instruction is for a greater-than-or-equal-to operation. It would have been obvious to one of ordinary skill in the art at the time the present invention was made to implement the teachings of Ben-Yoseph et al in order to compare the operands or data.

Claims 34-36, 41-43 and 47-49 are similar in scope to claims 9, 10, 17, 18, 20, 21, and 22, and thus are rejected under similar rationale.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kohn (5,155,816) teaches a pipelined apparatus and method for controlled loading of floating point data in a microprocessor.

Wickstrom et al (5,864,345) teaches a table based color conversion to different RGB16 formats.

Koyamada et al (5,956,041) teaches a method and device for volume rendering using concentric spherical slicing isosurfaces.

Responses

7. Responses to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231.

If applicant desires to fax a response, (703) **308-9051(52)** may be used for formal communications or (703) **308-5403** for informal or draft communications.

Please label "PROPOSED" or "DRAFT" for informal facsimile communications. For after final responses, please label "AFTER FINAL" or "EXPEDITED PROCEDURE" on the document.

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

Inquires

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Kee M. Tung** whose telephone number is (703) **305-9660**. The examiner can normally be reached on **Monday - Thursday** from **7:30 am to 5:00 pm**. The examiner can also be reached on alternate **Friday**.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Michael Razavi**, can be reached on (703) **305-4713**.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) **305-3800**.

June 23, 2000

Kee M. Tung
Primary Examiner
Art Unit 2776